

Design of a Model of a Single-Slope Integrated Type Voltage to Frequency Converter.

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ABSTRACT

The objective of this work is to design, construct, and implement a model of a single-slope integrating type voltage to frequency converter. The design was achieved with the help of a ramp generator, comparator, control logic, AND gate, counters, decoder, and display using electronic engineering design techniques. The method employed in the design was an adaptation of standard single-slope integrating type analogue to digital converter. The design utilized a low power rating of 4.8W instead of 6.0W which is presently in use. A bubble resolver was also included in the circuit to eliminate ± 1 error that is inherent in most digital devices. These modifications improved significantly the efficiency of the circuit even when the temperature changes during the operation of the model. The frequency (3.0Hz) obtained was consistent throughout the measurement. The model designed and constructed is capable of converting the analogue signal to digital signal, without losing meaningful information.

(Keywords: design, analogue/digital signals, modification adaptation)

INTRODUCTION

The integrating type of voltage to frequency converters is a device that converts analogue (voltage) to digital signal (frequency) without losing any meaningful information (Efedua, 2004). The linear ramp voltage is generated by charging a capacitor with constant current source; A D flip-flop is used to control this process.

The following conditions were deduce that; the converter output could be in error if:

- i. The analogue signal (V_{in}) level change appreciable during the

conversion time of the analogue to digital signal as with ADCs.

- ii. The capacitor charging current (I) varies during the conversion period.
- iii. There is a variation in clock frequency (f) for example due to temperature change.
- iv. There is also normal counting error of ± 1 1sb count associated with digital counters.

For a single slope analogue to digital integrating type to work satisfactorily it must overcome the conditions in (i-iv) above.

A list of components used in the design and the cost of the single-slope integrating type voltage to frequency converters are shown in Table 1 and Table 2 presents the measured results with reference voltage.

Table 1: Cost Estimate for the Design.

Components	QTY	Unit Price (N)	Total Price (N)
Transformer 240/12v	1	400	400
Diodes IN 4001	4	15	60
555 timer	1	60	60
Comparator/switch trigger	1	100	100
Counters (4510)	4	150	600
Decoder (4511)	4	150	600
Display	4	150	600
IC sockets (16 pins)	10	20	250
IC Sockets (8 pins)	2	20	40
Connecting wires	-	50	50
LEDs	2	10	20
Ramp generator	1	250	250
Capacitor	1	70	70
Total price			3,040

Table 2: Measured Results with Reference Voltage ($V_{ref}=10.5V$).

Test	Analogue signal (V_{in})			Digital Signal	Binary Equipment	Freq/No. of Pulses (Hz)
1	12.00	11.50	11.00	LLL	000	3
2	11.50	11.00	10.50	LLH	001	3
3	11.00	10.50	10.00	LHH	011	3
4	10.50	10.00	9.50	HHH	111	3

CONSTRUCTION DETAILS

The method employed in this design was an adaptation of standard single-slope integrating type analogue to digital converters although this method utilized low power rating of 4.8W instead of 6.0W (Efedua, 2004). D flip-flop (Bubble resolver) is included in the circuit to removed ± 1 error which inherent in most digital devices.

All components were mounted on a breadboard and tested for proper function before they were transferred to Vero board where construction was done stage-by-stage. The ramp generator was used as a triangular wave generator with constant current source; a 555 timer was used as an oscillator configured as a astable multi-vibrator to generate a gating pulse of constant time duration of 2s, which serves as the means of opening and closing of the AND gate so that the train of pulses coming from comparator output are counted by the counter. The comparator was used to compare the magnitude of the output voltage (V_o) and supply voltage (V_{cc}) to form a square wave. This stage was tested with oscilloscope in the laboratory to a certain the conversion of analogue to digital signal. The differentiator, time base, AND gate were used as a control circuit. A supply was connected to the main circuit as to start the circuit. After construction and calibration, the complete model was tested and measured up to 3.0Hz

Mode of Operation

Prior to the start of conversion, the control logic resets the ramp generator and the counter to zero. Thus at start of conversion the ramp voltage is zero and less than the analogue input voltage (V_{in}), hence the comparator output goes LOW, the condition is sense by the control logic which instructs the gate to open and allow the clock

pulse to pass through to be counted in every 2s; the signal voltage catches up with the input voltage, then the comparator goes HIGH and the control logic again instructs the gate to close. The counted output is decoded, processed and displayed as digital read out (frequency).

DESIGN METHODOLOGY

Brief Description of the Circuit

The circuit consist of ramp generator, bubble resolver (D-flip flop) oscillator (time base), logic gate, indicator and AND gate, counters, decoder, and display. The ramp generator output is connected to the input of the comparator; the output of oscillator/differentiator and the comparator are fed into the input of the bubble resolver at pin 3 and 2, respectively, where the input of the bubble resolver is connected to the counter then to the decoder. The differentiator output is connected to the counter for resetting the counter. The circuit diagram is shown in Figure 1.

Component Design

This stage took into consideration major components used in the design one by one as shown in Figure 1.

Power Supply

The power rating of the dc transformer was obtained as 4.8W from Equation (1) given by:

$$P=IV \quad (1)$$

where P is the power rating, while primary current was determine as 22mA from Equation (2) and IV are current and voltage, respectively.

$$I_p V_p = I_s V_s \quad (2)$$

where I_p is the primary current (Onohaebi, et al., 2006).

Ramp Generator

The ramp generator generates a constant current source that charge up the capacitor C_1 .

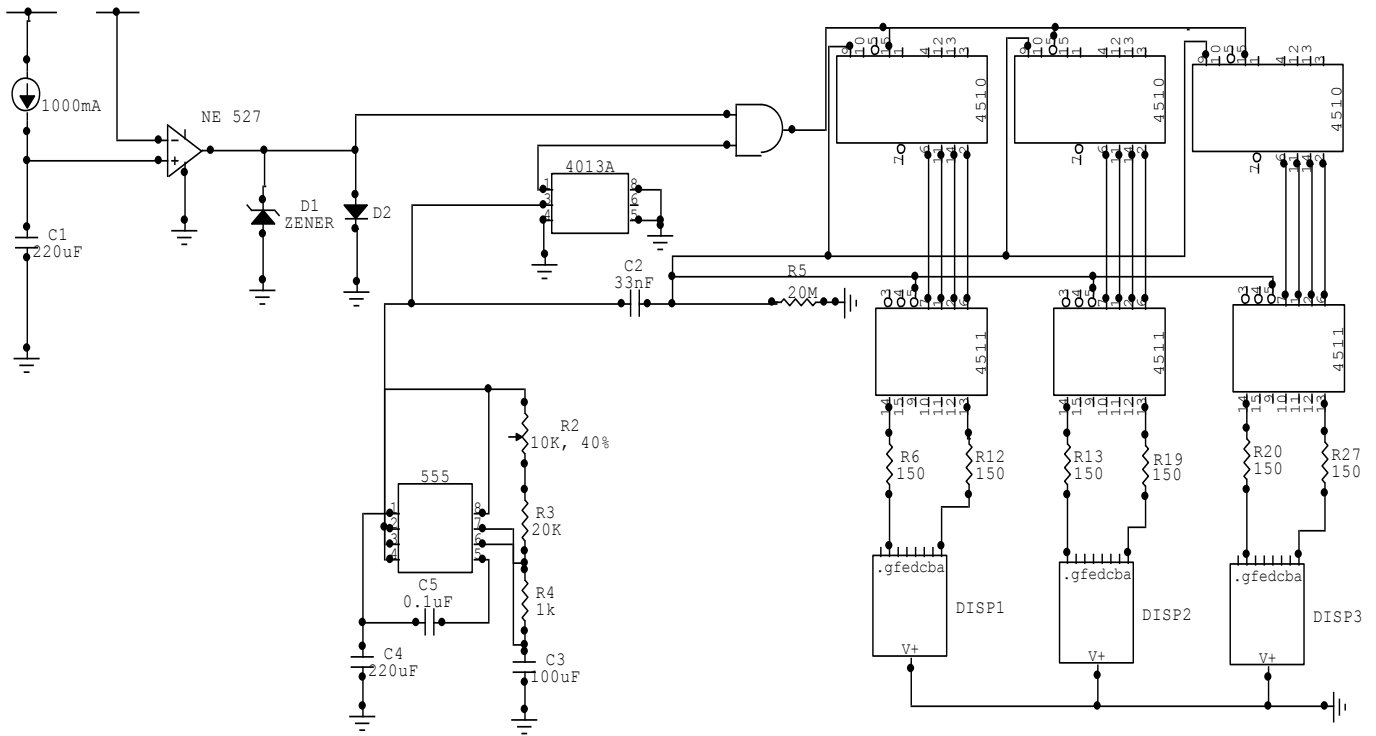


Figure 1: Circuit Diagram of a Single Slope Integrating Type Voltage to Frequency Converter.

The voltage when the C_1 is charged completed was obtained as $V_c=12V$ using Equation (3) given as:

$$V_c = \frac{1}{C_1} \int i dt \quad (3)$$

where i is the constant current source and V_c is the voltage required to charge up the capacitor completed (Robert, et al., 1999).

Comparator Stage

A comparator was used in this design to compare the time variable input voltage (V_{in}) with the V_{ref} with a view to determine whether $V_{in} \geq V_{ref}$. Although the V_{ref} determines the level at which comparison is made when the V_{in} exceeds V_{ref} , the comparator output takes on a value which is different in magnitude from when $V_{in} < V_{ref}$. A LOW (L) or HIGH (H) pulse is obtained from Equation (4) given as:

$$V_0 = V_{in} + V_{ref} \quad (4)$$

where V_0 is the output voltage which forms LOW or HIGH signal and V_{ref} is the reference voltage while V_{in} is the input voltage (Website, 2005b), for example if $V_{in} > V_{ref}$ the comparator takes on negative value which generates LOW pulses while if $V_{in} \leq V_{ref}$ the comparator takes on positive value which generates HIGH Pulses.

Time Base

It is used in this design as a stable multi-vibrator to generate a gating pulse of constant time duration of 2s. For the time base to generate the gating pulse; C_3 must charge up completely towards V_{cc} through the external resistor R_3 and R_4 so that the capacitor voltage rises above $2/3 V_{cc}$. This is the threshold voltage at pin 6, which derive the comparator to trigger the D flip-flop causing the output at pin 7 to discharge C_3 through R_4 . The period required when the gating pulses is HIGH, $T_H=2s$ and C_3 was obtained as 2509uF from Equation (5) given by:

$$T_H = 0.7(R_3 + R_4)C_3 \quad (5)$$

Thus C_3 chosen from data book to be $22\mu\text{F}$ as the next preferred value while the time taken when the gating pulses is low was obtained as $T_L = 0.18\text{s}$ from Equation (6) given by:

$$T_L = 0.7 R_4 C_3 \quad (6)$$

where T_L is the period when the gating pulse is LOW (Ronald, et al., 1999). Then the total time required when C_3 charge up and discharged completely was determined at $T = 2.18\text{s}$ from Equation (7):

$$T = T_L + T_H \quad (7)$$

where T is the total time required to charge and discharge the capacitor, (Website, 2005c), the frequency that oscillate the time base circuit was computed as $f_0 = 0.46\text{Hz}$ from Equation (8), given by:

$$f_0 = \frac{1}{T} \quad (8)$$

f_0 represents frequency of oscillator (Onuu, et al., 2006).

Control Logic (Differentiator) Circuit

This circuit is used in this design to reset the signal after each counting sequence, the differentiator is a short time type, however the voltage across the capacitor C_2 is zero and the clock frequency may equal to the frequency of the oscillation. C_3 was then obtained as 33.01nf from Equation (9); for practical purposes, C_3 was chosen as 33nF from the data book.

$$f = \frac{1}{2\pi R_5 C_2} \quad (9)$$

the diode D_1 indicates by coming ON each time a pulse is generated at the output of the comparator. Resistor R_1 was obtained from Equation (10) as 333Ω (Website, 2000a) but R_1 was chosen as 330Ω as the nearest value available value in the data book.

$$R_1 = \frac{V_{cc} - V_d}{i_d} \quad (10)$$

where V_d and i_d are diode drop and diode current respectively (Ali, 2006).

Operation of Bubble Resolver (D flip-flop)

The operation of the D flip-flop is very simple; it has synchronous control input: pin 1 will go to the same state that is present on pin 3, when the PGT occurs at clock. In other words, the level present at pin 3 will be stored in the flip flop at the instant of PGT occur. Assume that pin 1 is initially HIGH, when the first PGT occurs at point 'a' as in Figure 2, the D input pin 3 is LOW; thus pin 1 go to the 0 state.

Even though the level changes between 'a' and 'b' it has no effect on pin 1; pin 1 is storing the LOW that was on Pin 3 at point 'a' when the PGT at 'b' occurs pin d goes HIGH since pin 3 is HIGH at that time. Pin 1 stores the HIGH until the PGT at point 'c' cause pin 1 to go LOW since pin 3 is LOW at that time. Again it is important to notice that pin 1 can change when a PGT occurs. The pin 3 has no effect between PGTs.

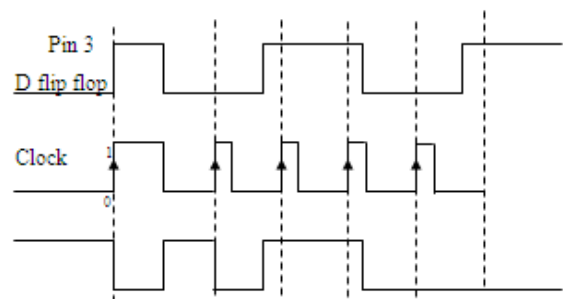


Figure 2: Wave Form of the Bubble Resolver (D – flip flop).

Reliability of the Model

If the parameter α and $R(t)$ are specified, we can find number of hours of operation when the model is put under stress. Assume that $\alpha = 0.01$ and $R(t) = 0.79$ the number of hours obtained when the model is put under stress is $t = 24\text{hrs}$ from Equation (11). After this period approximately 79% of the components of the model will fail.

$$t = -\frac{1}{\alpha} \ln R(t) \quad (11)$$

where R (t) is the reliability of the system and α =constant (Anazia, 2004).

PERFORMANCE TEST AND RESULTS

A signal generator was used in the laboratory to calibrate the time base unit to give precisely a gating pulse of constant time duration of 2s. Variable resistor R₂ was adjusted to confirm the accuracy of the calibration. After all necessary settings and adjustments were done, the model was enabled to convert analogue signals in triangular wave form to digital signals in square wave form with consistent frequency of 3Hz.

CONCLUSION

The design, construction, and implementation of a single slope integrating type analogue to digital converter was achieved despite highlighted assumptions and approximations. The design of the model cost about N3,050 which is five times less than the cost of an imported one. If this model can be developed by Nigeria industries it would tremendously reduce importation.

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